AMENDMENTS IN THE SPECIFICATION

Please replace paragraph [0007] with the following:

A major cost adder to the production of semiconductor devices (such as ASIC -- application-specific integrated circuit-- logic chips) is the time and financial costs incurred when testing the device. A major portion of the testing and associated costs involves the fusing process (i.e., the process by which the fuses are selected and electrically blown). Current electrical fusing times are on the order of [[200us]] 200µs per fuse. Due to the fusing current and on chip routing of relatively high voltage and high current busses, fusing multiple fuses at a time is not a practical solution for typical semiconductor devices. With fusing current as high as 15mA per fuse, multiple simultaneous fuse blow becomes difficult and requires more device I/O's to be dedicated to the fuse blow input (called FSOURCE) supply. Using many input pads on a chip/package to support electrical fusing is not a cost effective solution. Thus, fuses are currently blown in a serial manner (i.e., one at a time) during testing because of the high fusing current and other factors described. With electrical fuses it is desirable to reduce fusing time as much as possible.

Please replace paragraph [0016] with the following:

Since only a small percentage of the total number of fuses is to be blown during testing (e.g., 10 percent of the total number of fuses), a substantial time-savings is provided (i.e., almost 10X improvement for the example) by the invention with minimal circuit overhead. When serial readout of the fuse latches is required, the control signal is held low. This forces all the MUXes to select the high input and also forces all of the fuse latches to be in the shift path regardless of the state of the pattern latches. This forced non-bypass state can also be used for testing [[of]] the fuse latches where each latch needs to be in the shift path. Implementation of the invention thus reduces processing time for traditional eFuse circuit devices and testing procedures thereof.

Please replace paragraph [0029] with the following:

Figure 2 also illustrates possible inputs (signals and logic) to the device. Input circuitry and signals 210 provide the inputs required from powering and running/operating the eFuse circuits 220. Input circuitry and signals 210 include multiple clock signals, ACLK, BCLK, CCLK, gating logic, and a power source FSOURCE. Specific implementation of the input

circuitry and signals are not particularly important for the invention and conventional means may be utilized. However, in one embodiment of the invention, a specific configuration of input signals are provided for additional functionality, and this configuration of input signals is described within co-pending U.S. Patent Application, Serial No. [[XXX]] 10/604,908 (Attorney Docket Number BUR920030088US1, entitled "Method for Splitting Shift and Scan Paths on Scan Only LSSD Latches" and filed on [[June XX, 2003]] August 26, 2003. The relevant content of that application is hereby incorporated by reference.

Please replace paragraph [0029] with the following:

If the MUX selects the fuse latch input, a fuse blow process is indicated for the eFuse circuit as shown at block **431**, and fuse blow process is completed before the shifted 1 is passed to the next eFuse circuit. However, when the MUX does not select the fuse [[lath]] latch input, the MUX bypass input is selected and the shifted 1 is sent to the next eFuse circuit as shown at block **429**. The processing at the current eFuse circuit then ends, as shown at block **433**.

Please replace the paragraph [0037] with the following:

Figure 3B is a table showing the response of the MUX logic of Figure 3A to the select inputs of the AND logic and the clock time required for passing the shifted 1 through the sequence of eFuse circuits. The MUXes are indicated in each column and the parameter being tabulated [[in]] and shown in their respective rows, each entry now corresponding to the particular MUX. For illustrative purposes, it is assumed that a single clock cycle is required to complete a fuse blow operation at any one of the eFuse circuits at which the blow operation is completed. A bypass of the fuse blow operation is assumed to be almost negligible in terms of time (i.e., 1/100 of the time for the fuse blow). For a fuse with MUXes in bypass preceding it, the fusing time for that fuse will be reduced by the propagation delay of the MUXes. This however is negligible since the MUX delays are less than 1/4 nanosecond each and the fusing time is 200 microseconds.